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ELECTRICAL PROCESSES AND DEVICES FOR CONTROL OF PULSE DISCHARGE IN LIQUID MEDIUM

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Abstract

The realization of pulse discharge in liquid medium requires the usage of devices which can adapt the parameters of the supply network to the specifics of the load. For the development of such devices it should be possible to assess the controlled parameters and to define requirements for the elements in the respective circuits.

In the present work for an unified schematic solution are suggested models and analyses of the electrical processes is conducted. A comparison between the analytical and experimental results is done for a developed prototype.

Key words: *pulse discharge in liquid medium, systems for capacitive energy storage*

1. INTRODUCTION

PULSE WORKING MODE IN LIQUID MEDIUM

Devices for control of pulse discharge in liquid medium (DCPDLM), which realize pulse working mode consist of two relatively separate circuits, working in series in time:

- circuit for energy storage;
- discharge circuit.
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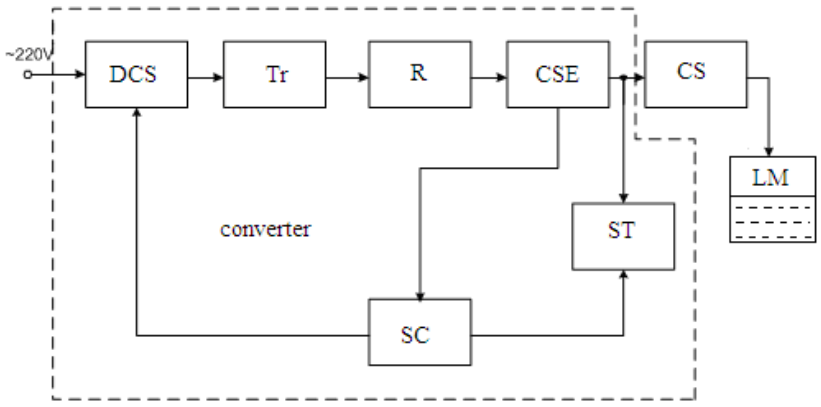


Fig.1 Block scheme of a device for control of pulse discharge in liquid medium /DCPDLM/

DCS - discharge control system;

Tr - transformer;

R - rectifier;

CSE - capacitive storage element (work capacitor);

ST - stabilizer of the work capacitor voltage;

CW - controlled switch;

LM - liquid medium;

SC - system for control..

Different methods for energy storage are known in literature: stored in capacitors, inductive coils; electrochemical methods, etc. At presence, the most commonly used in DCPDLM are systems for capacitive energy storage. They should meet the following requirements:

- necessity for regulations of the stored energy in a wide range, as the charging time is limited by the required frequency of the discharge pulses;
- possibility for short time work in a mode close to short circuit because at the moment of discharge formation the resistance of the liquid medium is very small /less than 1 ohm/;
- charging voltage stabilization for ensuring repeatedness of the generated pulses. It is appropriate to be used parallel compensation stabilizers connected directly to the work capacitor as well as predischarge circuits when low frequencies of the discharge pulses.
- limitation of the charge current with different current-limiting reactive elements.

A circuit for energy storage can be presented as a converter with an input and an output. An analysis of such converter including its structure and the relations between the input and output parameters is missing in literature.

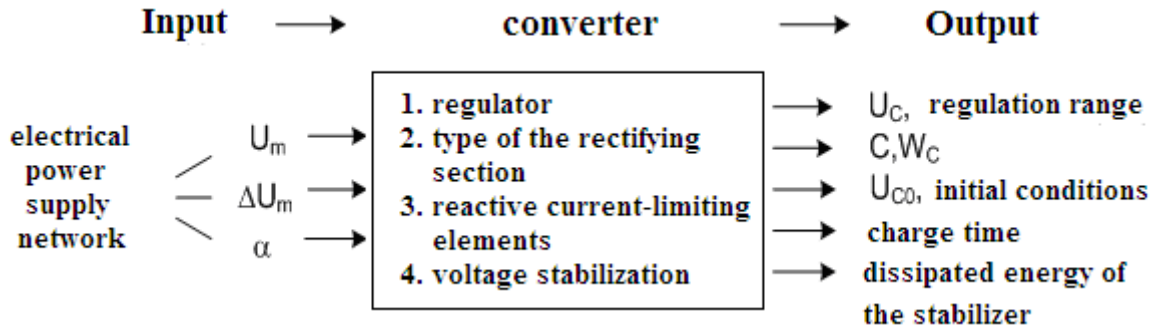


Fig. 2 Charge circuit

where:

- U_m, ΔU_m – amplitude and alteration of the input voltage
- α – conductivity angle of the regulator
- C, W_C – capacitance and energy of the capacitive battery
- ΔU_{C0} – initial charge voltage

II. RESEARCH TASKS

On the basis of the mentioned specifics the following tasks can be defined:

1. development of an unified scheme of a converter in the circuits for capacitive energy storage on the basis of:

- step-up transformer with dissipation and alternative current regulator in low voltage side;
- rectifying sections with capacitive current limiting such as a capacitor in a non-symmetrical voltage doubler in the rectifying section or additional added capacitive current limiting element;
- parallel stabilizer to the work capacitor battery.

2. development of model for analysis of the electrical processes including the structure of the converting section, its input parameters – amplitude and variation of the input supply voltage and the conductivity angle of the AC regulator. The model should give possibilities for:
    - defining of the controlled parameters such as charging time for the corresponding charge voltage in the regulated range, dissipated energy by the parallel stabilizer, instability of the charge voltage.
    - defining of the elements loading of the converter.
3. development of a model of the discharge circuit for defining of the discharge pulse parameters – amplitude, shape, duration;

III. ANALYSES OF CIRCUITS FOR CAPACITIVE ENERGY STORAGE

On fig.3 is shown a variant for a power circuit, which should meet the requirements of the charge process.

The transformer is presented as: a voltage source - U_m, resistance of the transformer windings $R_в$ and inductance L. On the primary side of the transformer there is a symistor ST, which is used to switch (on and off) the supply voltage. The rectifier is full-wave – Gretz scheme and consists of the diodes $D_1 \div D_4$. The parallel voltage stabilizer is presented with a resistor connected in series R with ideal switch Sw and both connected in parallel with a storage capacitor C.

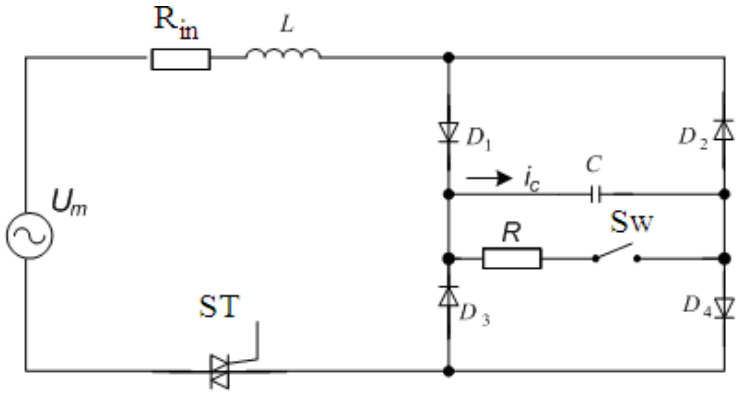


Fig.3 A circuit for capacitive energy storage with a bridge rectifier – Gretz

The parallel stabilizer is used to discharge C when the given charging voltage of the capacitor is exceeded. The limitation of the maximum charging current $I_{CH.max.}$ is set by the inductance L and the internal resistance of the windings R_{in}.

If we accept the diodes and the symistor for ideal elements, the development of the charging process in time can be followed on fig. 4,5 and 6. The curves refer to certain values – R_{in}=140,Ω, L=0,8,H, C=100,μF и U_m=2820,V.

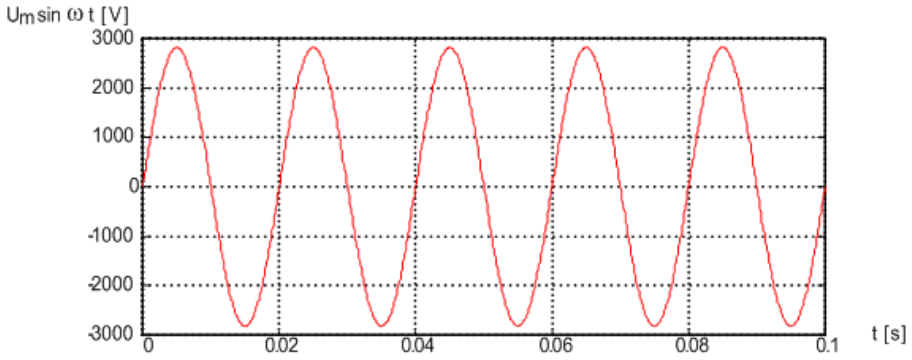


Fig. 4 Input sinusoidal voltage

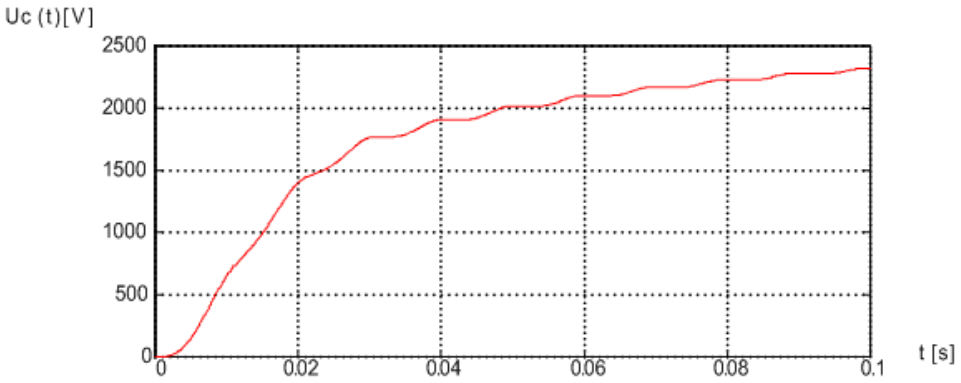


Fig.5 Time diagram of the capacitor charging voltage

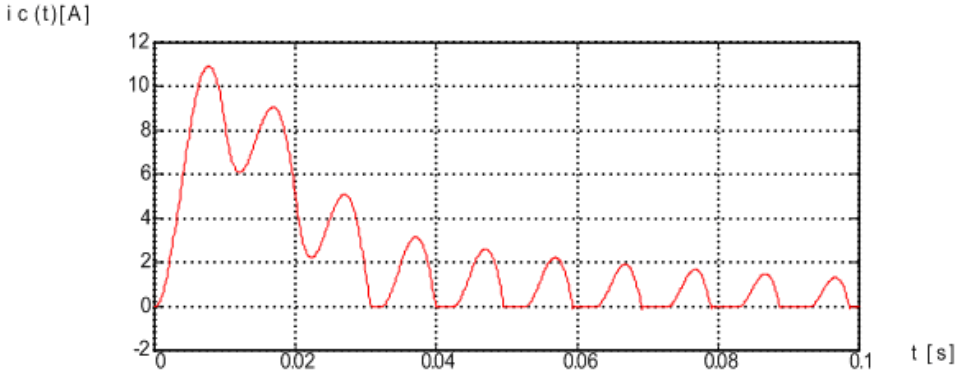


Fig.6 Time diagram of the charging current of the capacitor

One of the main parameters for the design of a DPDLM is the charging time t_{CH}, which defines the frequency of the discharge pulses. The charging time depends on different factors $t_{CH}= t_{CH}(R_{in}, L, U_m, C)$. The influence of these parameters C, L и U_m with certain values over the charging time is shown on fig.7, 8 and 9.

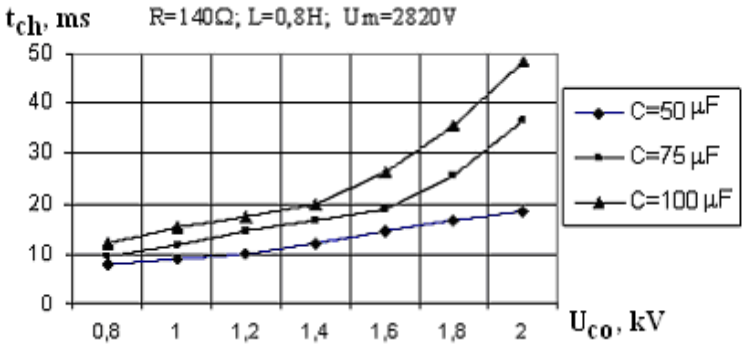


Fig.7

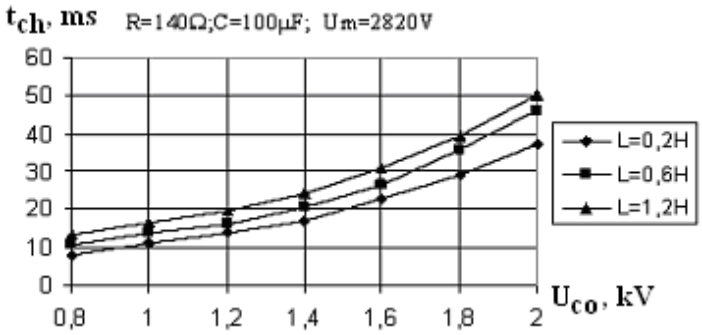


Fig.8

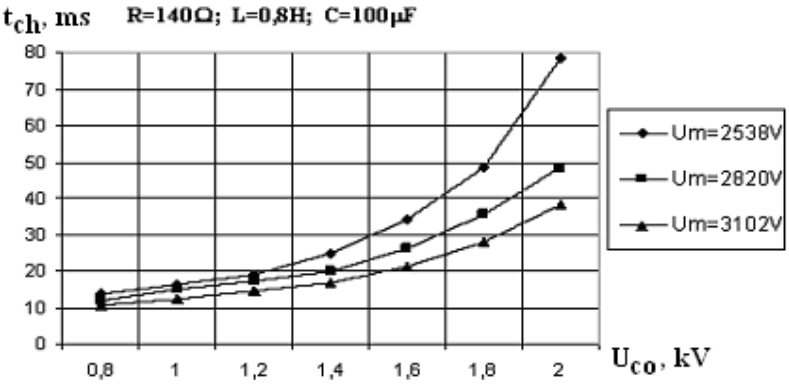


Fig.9

Charging time depending on the main parameters of the charging circuit – Gretz scheme

The limitation of the charging current can be done by adding reactive elements in the alternative current part of the rectifying section – Fig.10.

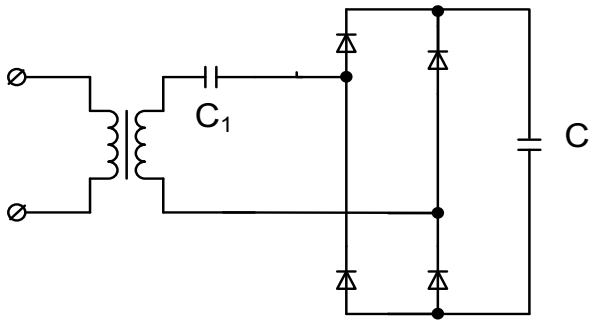


Fig.10 Circuit for capacitive energy storage with reactive current limiting element – capacitor

For R_{in}=1040 Ω, C_1=1 μF, C=2 μF, L=0,8 H, aand U_m=28,2 kV the development of the charging processes can be followed on fig.11, 12, 13 and 14. Fig.15, 16 and 17 show the dependency $t_{ch}=t_{ch}(C, C_1, U_m)$. From the conducted researches it can be concluded that for L=0,2÷1,2 H – t_{ch} almost doesn't change.

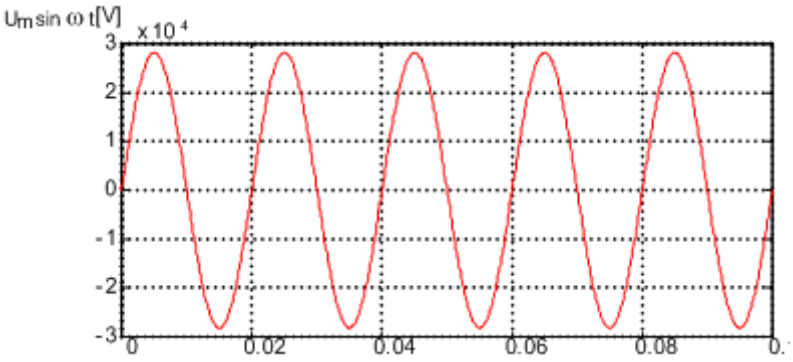


Fig.11

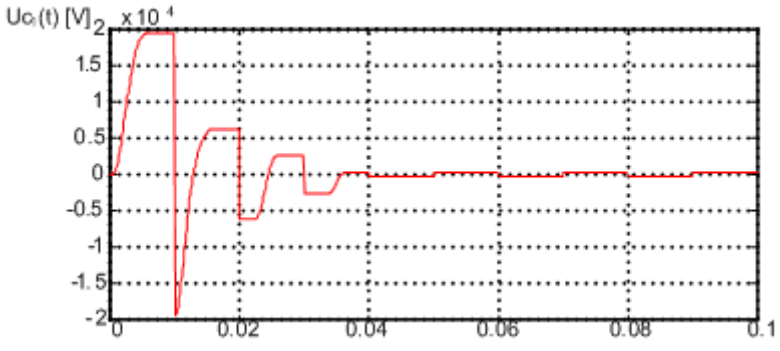


Fig.12

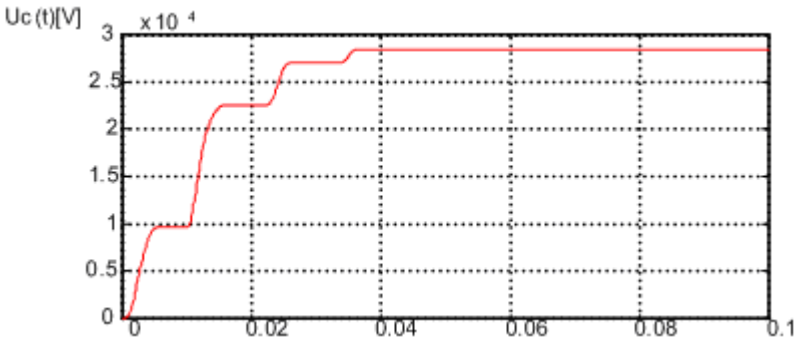


Fig.13

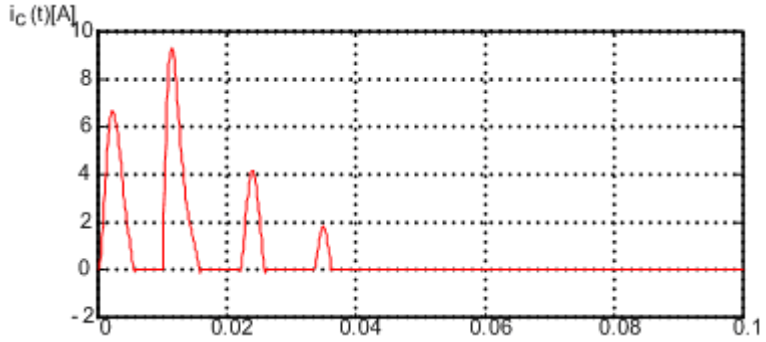


Fig14

Time diagrams of the development of the charging process in circuits with capacitive current limiting and Gretz rectifier scheme - L=0,8 H; R=1040 Ω; C_1=1 μF и C=2 μF

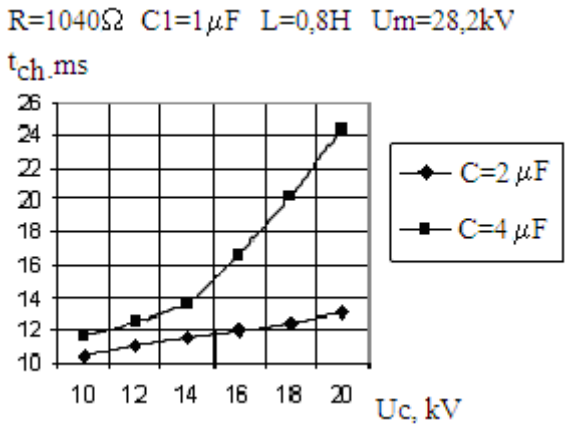


Fig.15

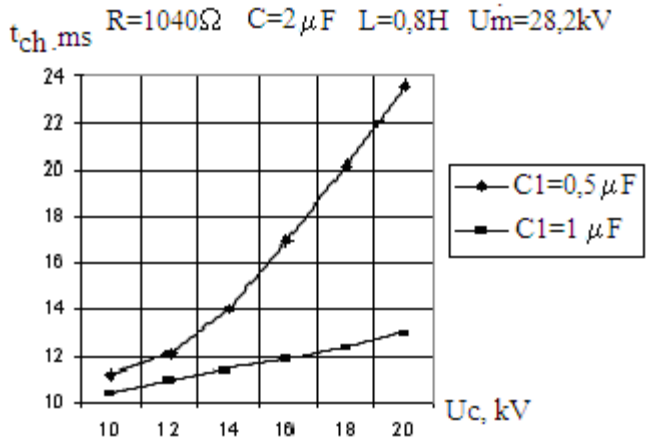


Fig.16

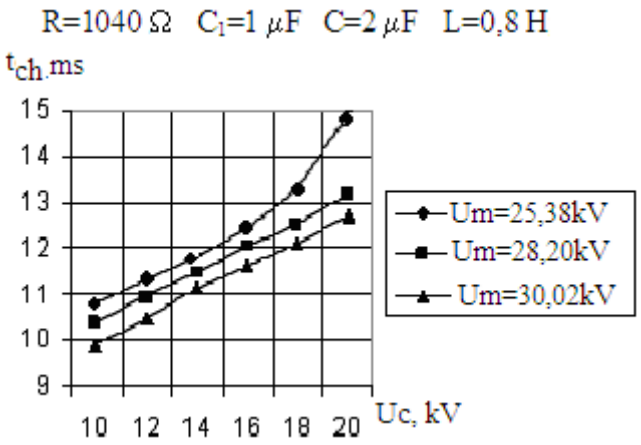


Fig.17

Charging time as a function of the main parameters of the charging circuit with capacitive current-limiting element

The usage of a capacitive current-limiting element is typical for the schemes of voltage multipliers – fig.18. The charging process is described with fig.19 and equations 1÷11 [5]:

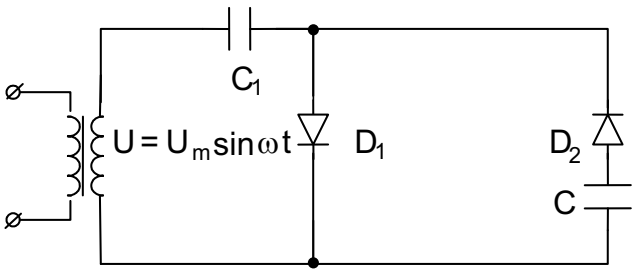


Fig. 18 A circuit for capacitive storage based on a voltage doubler

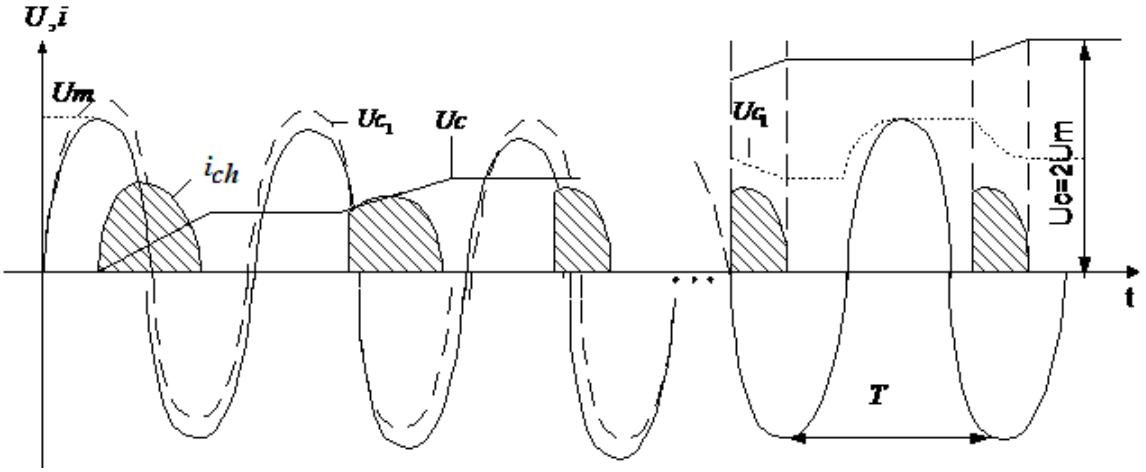


Fig. 19 Charging process in a voltage doubler

For a random moment in the n-th pulse of charging the capacitor C is valid equation 1:

$$u_{Cn} + u_{C1n} = u = U_m \sin(\omega t + \varphi_n) \tag{1}$$

where: φ_n is the phase shifting of the moment of turning on the diode.

After differentiating equation 1:

$$i_{chn} = C\frac{du_{Cn}}{dt} = C_1\frac{du_{C1n}}{dt} \tag{2}$$

Then, the charging current, when D_2 is conductive, is defined with equation 3:

$$i_{chn} = U_m \omega \frac{C_1.C}{C_1 + C}\cos(\omega t + \varphi_n) \tag{3}$$

At the moment of turning on the diode D_2:

$$|u_{Cn}(0)| - |u_{C1}(0)| = U_m \sin\varphi_n \tag{4}$$

Because at this moment $u_{C1n}(0) = U_m$, it follows that:

$$u_{Cn}(0) - U_m = U_m \sin\varphi_n \tag{5}$$

from where:

$$\sin\varphi_n = \frac{u_{Cn}(0)}{U_m} - 1 \tag{6}$$

The voltage u_{Cn} at the moment of passing the n^{-th} pulse of the charging current can be defined by equation 7:

$$u_{Cn} = \frac{1}{C}\int i_{3n}dt = \frac{U_m C_1}{C_1 + C}\sin(\omega t + \varphi_n) + K$$

K is a integrating constant and is defined by the border conditions.

The charging current arises at $\omega t = 0$ and becomes 0 at $\omega t + \varphi_n = \pi/2$.

$$\left.\begin{aligned} u_{Cn}(0) &= \frac{U_m C_1}{C_1 + C}\sin\varphi_n + K \\ u_{Cn+1}(0) &= \frac{U_m C_1}{C_1 + C} + K \end{aligned}\right\} \tag{7}$$

Replacing $\sin\varphi_n$ from equation 6 in equation 7, it can be determined the capacitor charging voltage in the n-th interval of charging – equation 8:

$$\Delta u_{Cn} = u_{Cn+1}(0) - u_{Cn}(0) = \frac{C_1}{C + C_1}\left[2U_m - u_{Cn}(0)\right] \tag{8}$$

After transformation of equation 8:

$$\frac{u_{Cn+1}(0)}{2U_m} = 1 - (1 - A)\left[1 - \frac{u_{Cn}(0)}{2U_m}\right] \tag{9}$$

where $A = \frac{C_1}{C_1 + C}$. Then:

$$\frac{u_{C2}(0)}{2U_m} = 1-(1-A)$$

$$\frac{u_{C3}(0)}{2U_m} = 1-(1-A)^2$$

$$\frac{u_{Cn}(0)}{2U_m} = 1-(1-A)^{n-1} \tag{10}$$

where $n-1 = \frac{t}{\Delta t} = \frac{\omega t}{\pi}$ - previous intervals of charging.

On fig.20 is shown the change of $\frac{u_C(0)}{2U_m} = f(n)$

The pulse amplitude of the charging current can be defined with equation 11:

$$I_{chm} = U_m \omega \frac{C_1.C}{C_1 + C} \tag{11}$$

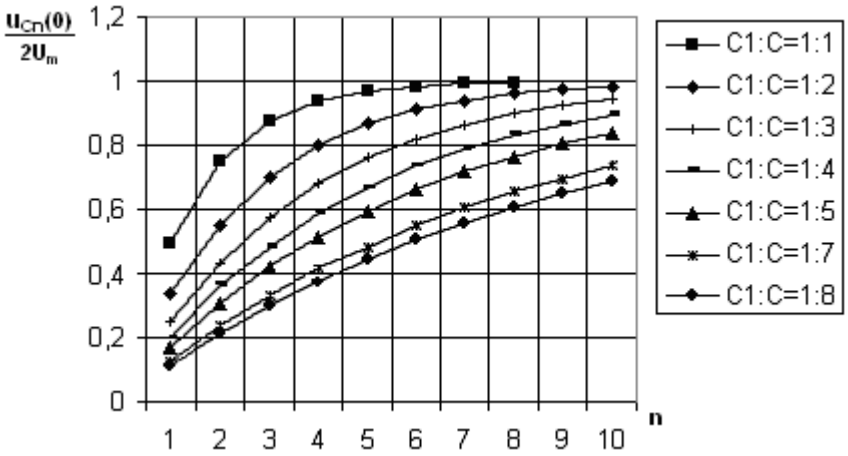


Fig.20 Voltage increase for the first 10 periods as a function of the ratio between the current-limiting and the main capacitors

In the suggested analytical model are not considered the following:

- the parameters R_{in} and L of the transformer on the input of the doubler and fig.18;
- the differences of the charging process depending on which diode D1 or D2 is turned on during the first half-wave of the charging process.

The question about the non-zero initial conditions for the charging process is also not cleared out. The process is modeled with a system of differential equations (for a complicated circuit including the parallel stabilizer – fig.12 and 13). After solving this system for one particular variant R_e=520 Ω, C_1=1 μF, C=2 μF, L=0,9 H, U_m=14 kV the development of the charging process is presented on fig.21÷24. The dependency $t_{ch}=t_{ch}(C, C_1, U_m)$ is shown on fig.25÷27. In that case t_{ch} depends slightly on the change of L in the range 0,5÷1 H.

When comparing the results from fig.20 and fig.23 it can be seen that the difference is smaller than 20% i.e the analytical expressions with certain approximation can used for determination of the charging circuits elements presented as a voltage doubler with the absence of a thyristor AC regulator in the input of the step-up transformer.

The usage of thyristors and symistors allows switching on and off and possibility for passing through parts of the input sinusoidal voltage. Both the thyristors and the symistors are not fully controllable elements. Their triggering (on state) is induced by a control pulse and they switch off when the current which passes through them becomes 0. This way of switching off especially in circuits with inductivities presumes lower level of the commutation overvoltages.

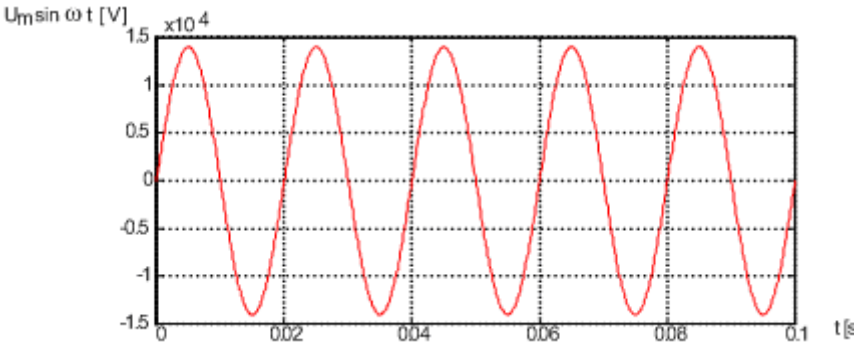


Fig.21

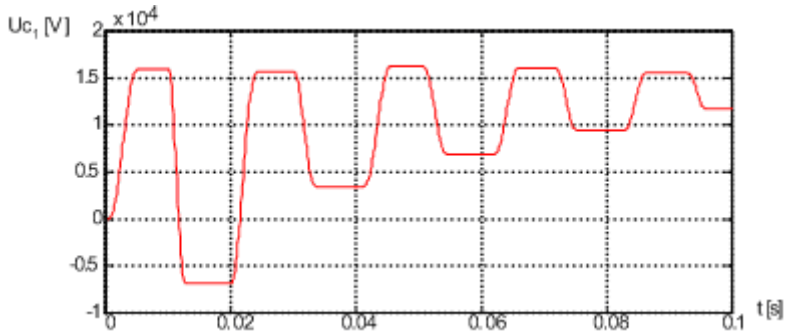


Fig.22

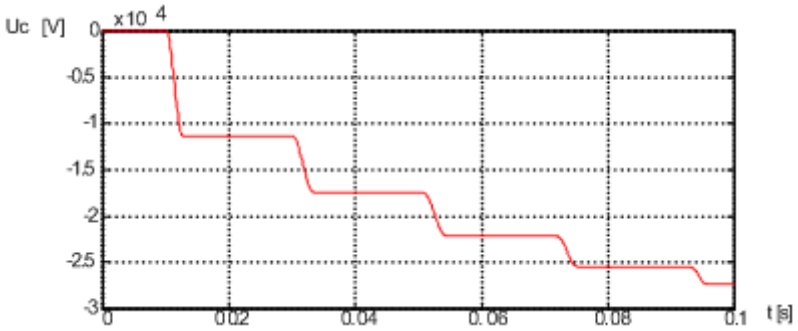


Fig.23

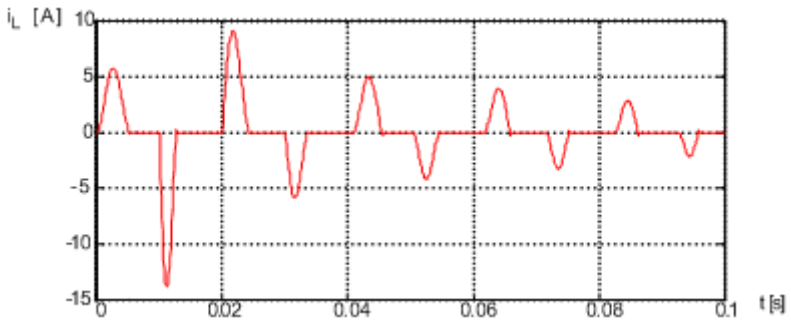


Fig.24

Time development of the charging process in a circuit of a voltage doubler for L=0,9 H; R=520 Ω; C_1=1 μF and C_2=2 μF

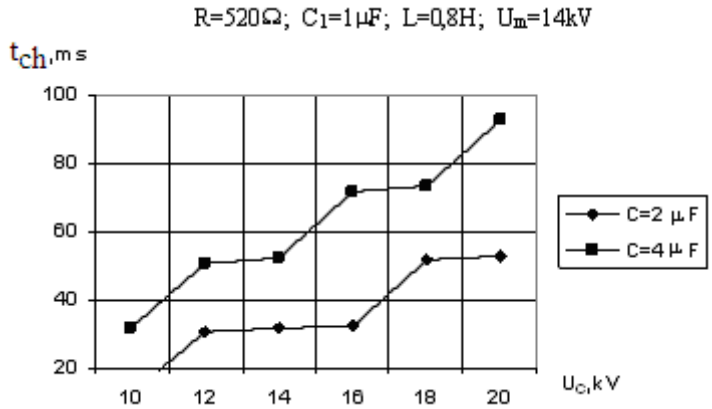


Fig.25

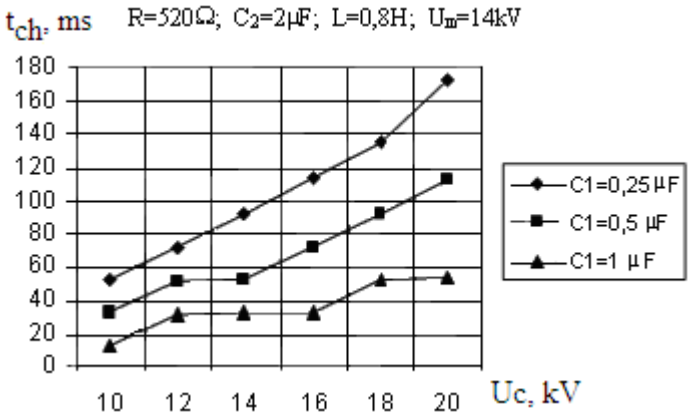


Fig.26

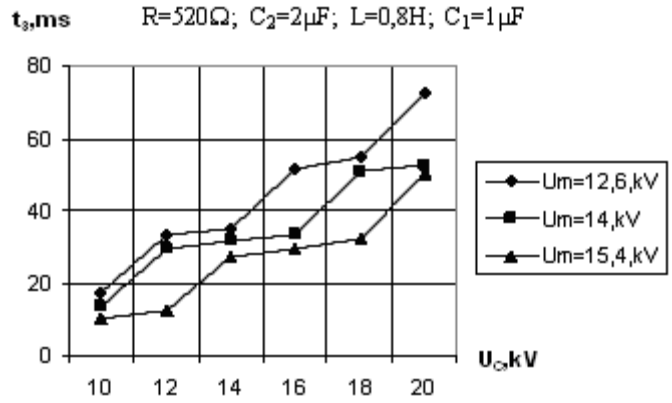


Fig.27

Dependency of the charging time in a circuit with a doubler from the parameters of the charging circuit

However, the usage of thyristors and symistor would bring to charging the capacitor battery over the necessary voltage at the expense of their conductivity in the respective half-period after stopping the control pulses. This overcharging also defines the dissipated power of the parallel stabilizer. If a rectifier (arranged as a doubler) is used, the equivalent scheme of the converter with capacitive energy storage looks like fig.28, where:

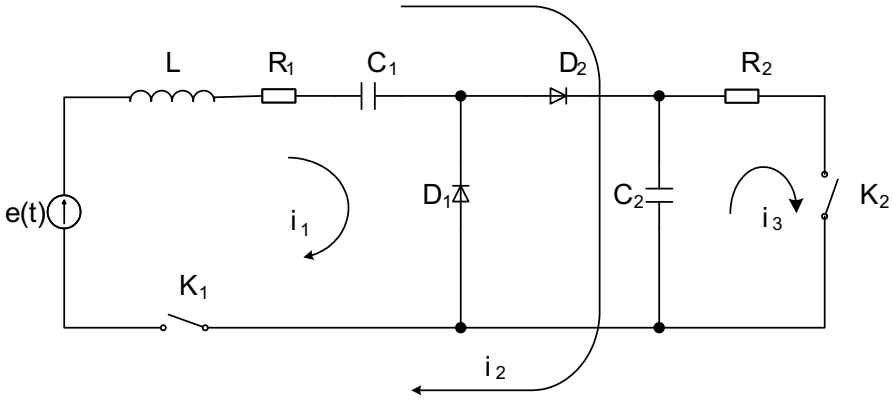


Fig.28 Equivalent scheme of a system for capacitive energy storage, realized as a doubler with control switch in the AC side and parallel stabilizer in the DC side

- e(t) is the voltage of the secondary side of the input transformer
- L and R_1 are the inductivity and resistance of the secondary winding of the transformer
- K_1 – a switch representing a symistor or thyristor switch
- R_2, K_2 – parallel stabilizer

The assumptions that the transformer can be presented only with e(t), L and R_1, i.e. without considering: the losses in the steel; that the switches in the AC and DC circuits are ideal and that the time constant in the control circuit of the symistor is sufficiently high i.e. the control angle α is constant during the charging process.

The circuit from fig.28 can be analyzed by the method of conditional variables.

In the time domain can be formed several intervals:

- Interval 1 – beginning of the charge process – D_1 is conductive (fig.28) and C_1 is charging. The interval is shown on fig.29 in the limits $t_1 \le t \le t_2 + \varepsilon_1$, where t_1 is the moment when the symistor is triggered into the forward conduction zone/switched on/, represented with the switch K_1, and $t_2 + \varepsilon_1$ is the moment of commutation of the symistor when the currents becomes 0.
- Interval 2 - $t_3 \le t \le t_4 + \varepsilon_2$ - The diode D_2 is conductive and C_2 is charging.- fig.28.

  Intervals 1 and 2 are repeating in a cycle and the capacitor C_2 is charging.
- Interval "n" - $t_3^n \le t \le t_4^n + \varepsilon_2^n$. During this interval at a moment t_e ($t_3^n \le t_e \le t_4^n + \varepsilon_2^n$), C_2 is charging to a previously set voltage, the switch K_2 – fig.28 - closes and C_2 starts to discharge through R_2 and K_2, which compensates the overcharge for the time interval $t_e \div t_4^n + \varepsilon_2^n$.

The time intervals are shown on fig.29.

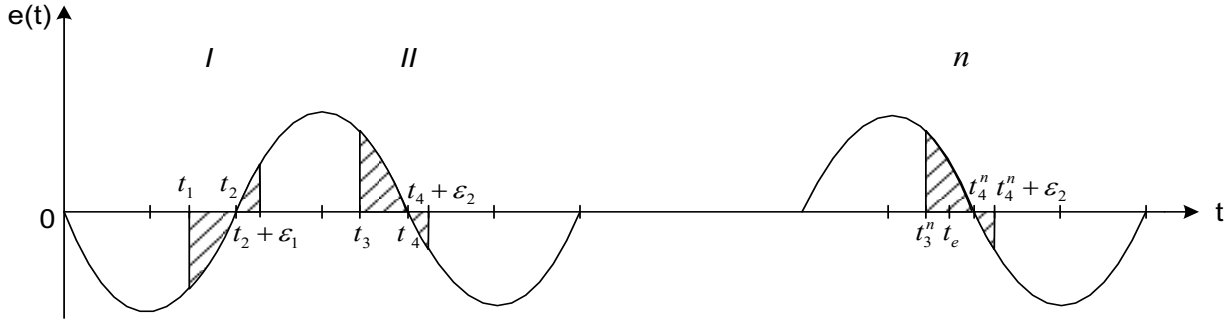


Fig.29 Charging process of a doubler in the time domain

Interval 1: $t_1 \le t \le t_2 + \varepsilon_1$; K_1 – closed, K_2 – open. The scheme from fig.28 is transformed into fig.30.

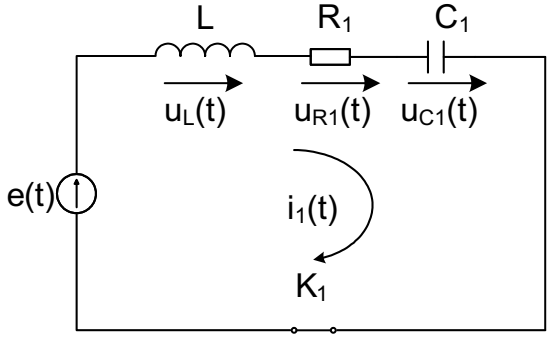


Fig.30 Equivalent scheme for Interval 1

The system of equations for fig.30 is (12):

$$\begin{cases} L\dfrac{di_1(t)}{dt} + R_1 i_1(t) + u_{C_1}(t) = e(t) \\ C_1\dfrac{du_{C_1}(t)}{dt} = i(t) \end{cases} \tag{12}$$

The initial conditions are the following:

- $i_1(t_1+) = i_1(t_1-) = 0$
- $u_{C_1}(t_1+) = u_{C_1}(t_1-) = 0$

- $u_{C_2}(t_1+) = u_{C_2}(t_1-) = 0$

After normalizing, the system (12) is transformed into (13) and in a matrix form – equation (14):

$$\left| \begin{array}{l} \dfrac{du_{C_1}(t)}{dt} = \dfrac{1}{C_1} i_1(t) \\ \\ \dfrac{di_1(t)}{dt} = -\dfrac{u_{C_1}(t)}{L} - \dfrac{R_1}{L} i_1(t) + \dfrac{e(t)}{L} \end{array} \right. \tag{13}$$

$$\frac{d}{dt}\begin{bmatrix} u_{C_1}(t) \\ i_1(t) \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{C_1} \\ -\dfrac{1}{L} & -\dfrac{R_1}{L} \end{bmatrix} \begin{bmatrix} u_{C_1}(t) \\ i_1(t) \end{bmatrix} + \begin{bmatrix} 0 \\ \dfrac{1}{L} \end{bmatrix} . [e(t)] \tag{14}$$

$$[x_1(t)] = \begin{bmatrix} u_{C1}(t) \\ i_1(t) \end{bmatrix} = [x_1(t_1+)] e^{[A_1].(t-t_1)} + e^{[A_1].t} . \int_{t_1}^{t} e^{-[A_1].\tau} . [B_1][f(\tau)] d\tau \tag{14a}$$

where

$$[A_1] = \begin{bmatrix} 0 & \dfrac{1}{C_1} \\ -\dfrac{1}{L} & -\dfrac{R_1}{L} \end{bmatrix}; \quad [B_1] = \begin{bmatrix} 0 \\ \dfrac{1}{L} \end{bmatrix}; \quad [f(\tau)] = [e(t)] \quad :$$

The precise solution is according to the formula of Cauchy. The final conditions i.e. $u_{C_1}(t)$ and $i_1(t)$ at the moment $t = t_2 + \varepsilon_1$ are as follows:

$$[x_1(t_2+\varepsilon_1)] = \begin{bmatrix} u_{C_1}(t_2+\varepsilon_1) \\ i_1(t_2+\varepsilon_1) \end{bmatrix} = \begin{bmatrix} u_{C_1}(t_2+\varepsilon_1) \\ 0 \end{bmatrix} \tag{15}$$

Interval 2: $t_3 \le t \le t_4 + \varepsilon_2$. The equivalent scheme on fig.28 is transformed into fig.31 For the circuit on fig.31 is the valid equation (16).

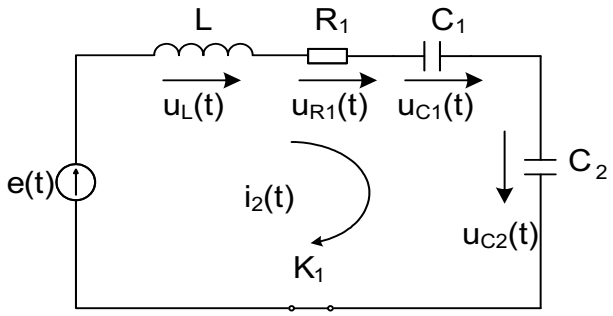


Fig.31 Equivalent scheme for Interval 2

$$\frac{d}{dt}\begin{bmatrix} u_{C_2}(t) \\ u_{C_1}(t) \\ i_2(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_2} \\ 0 & 0 & \frac{1}{C_1} \\ -\frac{1}{L} & -\frac{1}{L} & -\frac{R_1}{L} \end{bmatrix} \begin{bmatrix} u_{C_2}(t) \\ u_{C_1}(t) \\ i_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L} \end{bmatrix} [e(t)] \tag{16}$$

The solution of equation (16) looks like:

$$[x_2(t)] = \begin{bmatrix} u_{C2}(t) \\ u_{C1}(t) \\ i_2(t) \end{bmatrix} = [x_2(t_3+)] e^{[A_2](t-t_3)} + e^{[A_2]t} \cdot \int_{t_3}^{t} e^{-[A_2]\tau} \cdot [B_2][f(\tau)] d\tau \tag{16a}$$

where:

$$[A_2] = \begin{bmatrix} 0 & 0 & \frac{1}{C_2} \\ 0 & 0 & \frac{1}{C_1} \\ -\frac{1}{L} & -\frac{1}{L} & -\frac{R_1}{L} \end{bmatrix}; \quad [B_2] = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L} \end{bmatrix}; \quad [f(\tau)] = [e(t)]$$

$$[x_2(t_3+)] = \begin{bmatrix} u_{C_2}(t_2+\varepsilon_1) \\ u_{C_1}(t_2+\varepsilon_1) \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ u_{C_1}(t_2+\varepsilon_1) \\ 0 \end{bmatrix} \tag{17}$$

At moment $t = t_4 + \varepsilon_2$ the current $i_2(t)$ becomes equal to 0. The final conditions i.e. the values of $u_{C_2}(t)$, $u_{C_1}(t)$ and $i_2(t)$ when $t = t_4 + \varepsilon_2$ are the following:

$$\left[x_2\left(t_4+\varepsilon_2\right)\right]=\begin{bmatrix}u_{C_2}\left(t_4+\varepsilon_2\right)\\ u_{C_1}\left(t_4+\varepsilon_2\right)\\ i_2\left(t_4+\varepsilon_2\right)\end{bmatrix}=\begin{bmatrix}u_{C_2}\left(t_4+\varepsilon_2\right)\\ u_{C_1}\left(t_4+\varepsilon_2\right)\\ 0\end{bmatrix} \tag{18}$$

We accept that at moment t_e from the n[th] interval capacitor C_2 charges to the defined voltage. Then, the switch K_2 closes and it begins compensation of the overvoltage of C_2 after the moment t_e i.e. the discharge through the switch K_2 and the resistor R_2 – fig.33. Hence, the n[th] interval can be divided into two parts:

- $t_3^n \le t \le t_e$
- $t_e \le t \le t_4^n + \varepsilon_2^n$

For the interval $t_3^n \le t \le t_e$ is valid equation (6), which initial conditions are set with equation (19).

$$\left[x_2\left(t_3^n+\right)\right]=\begin{bmatrix}u_{C_2}\left(t_3^n+\right)\\ u_{C_1}\left(t_3^n+\right)\\ i_2\left(t_3^n+\right)\end{bmatrix}=\begin{bmatrix}u_{C_2}\left(t_4^{n-1}+\varepsilon_2^{n-1}\right)\\ u_{C_1}\left(t_2^n+\varepsilon_1^n\right)\\ 0\end{bmatrix} \tag{19}$$

The final conditions are defined at a moment $t=t_e-$:

$$\left[x_2\left(t_e-\right)\right]=\begin{bmatrix}u_{C_2}\left(t_e-\right)\\ u_{C_1}\left(t_e-\right)\\ i_2\left(t_e-\right)\end{bmatrix}=\left[x_2\left(t_e+\right)\right]=\begin{bmatrix}u_{C_2}\left(t_e+\right)\\ u_{C_1}\left(t_e+\right)\\ i_2\left(t_e+\right)\end{bmatrix} \tag{20}$$

For the interval $t_e \le t \le t_4^n + \varepsilon_2^n$ the equivalent scheme in fig.28 looks like the circuit in fig.32:

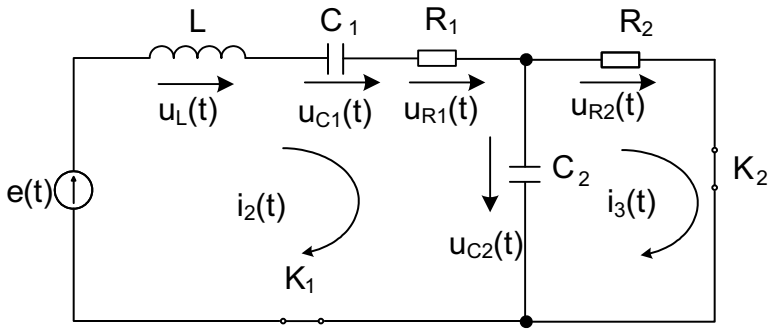


Fig.32 Equivalent scheme for the n-[th] Interval

For the circuit in fig.32 $i_3(t)=\frac{u_{C_2}(t)}{R_2}$ and equation (21) is in force:

$$\frac{d}{dt}\begin{bmatrix} u_{C_2}(t) \\ u_{C_1}(t) \\ i_2(t) \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_2C_2} & 0 & \frac{1}{C_2} \\ 0 & 0 & \frac{1}{C_1} \\ -\frac{1}{L} & -\frac{1}{L} & -\frac{R_1}{L_1} \end{bmatrix} \begin{bmatrix} u_{C_2}(t) \\ u_{C_1}(t) \\ i_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L} \end{bmatrix} [e(t)]. \tag{21}$$

Its solution looks like:

$$[x_2(t)] = \begin{bmatrix} u_{C2}(t) \\ u_{C1}(t) \\ i_2(t) \end{bmatrix} = [x_2(t_e+)]e^{[A_3].(t-t_e)} + e^{[A_3].t}.\int_{t_e}^{t} e^{-[A_3].\tau}.[B_3][f(\tau)]d\tau \tag{21a}$$

where:

$$[A_3] = \begin{bmatrix} -\frac{1}{R_2C_2} & 0 & \frac{1}{C_2} \\ 0 & 0 & \frac{1}{C_1} \\ -\frac{1}{L} & -\frac{1}{L} & -\frac{R_1}{L} \end{bmatrix}; \quad [B_3] = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L} \end{bmatrix}; \quad [f(\tau)] = [e(t)]$$

The solution is according to the Cauchy equation.

The beginning and the end of the charge process are shown on fig.33 using MATLAB to visualize the conductivity angle $\alpha = 1,9rad; L = 50H; R_1 = 3k\Omega; C_1 = 0,25\mu F; C_2 = 1\mu F$ and $R_2 = 30k\Omega$.

The method of description of the charge circuit allows introduction of non-zero initial conditions.

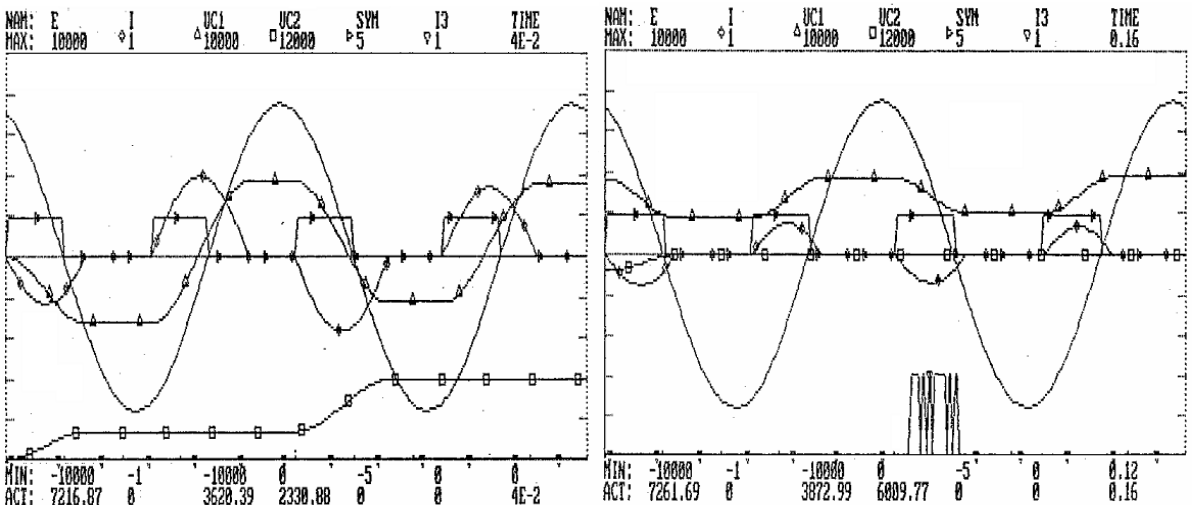


Fig.33

An example realization of the charging circuit from fig.28 is shown on fig.34, where:

– Tr – step-up transformer.

– S - symistor

– C_1, C_2 and D_1, D_2 – voltage doubler

– L_1, T_1 – lamp-transistor switch of the parallel stabilizer. When triggering the switch (conducting mode) the current through it is limited by R_2. Usually the current through R_2, L_1, T_1 should be bigger than charging current through C_2 to ensure compensation of the overcharging of C_2 and stabilization of U_{C2}.

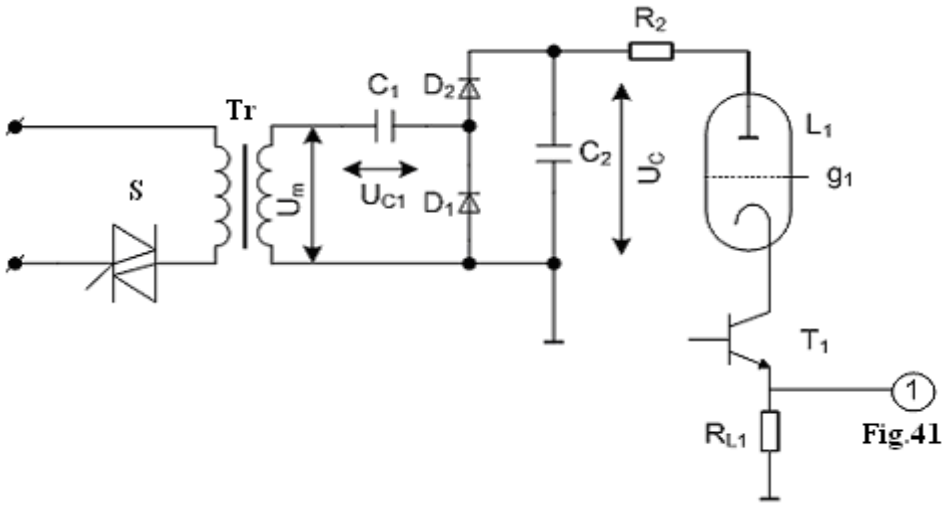


Fig.34 Charging circuit with control in the AC and DC sides

With the such determined current through the parallel stabilizer, it works in a pulse mode. If U_{C0} is the voltage which the C_2 is charged to, the parallel stabilizer switches on when $U_{C2}>U_{C0}$. It follows: compensation of the overcharge, switching off when $U_{C2}=U_{C0}$, new overcharging, switching on, new compensation of the discharge and so on – fig.33 – current I_{ch}.

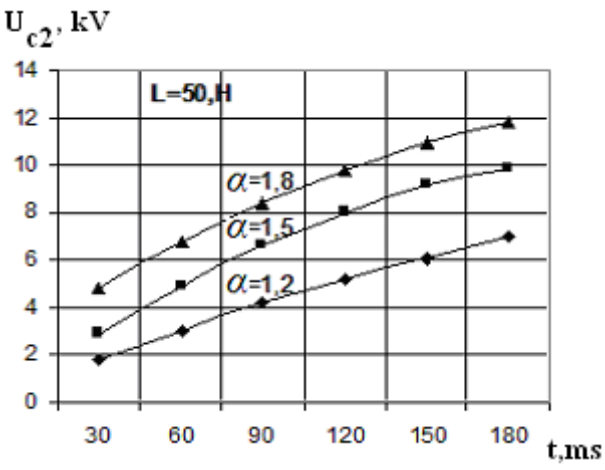


Fig.35

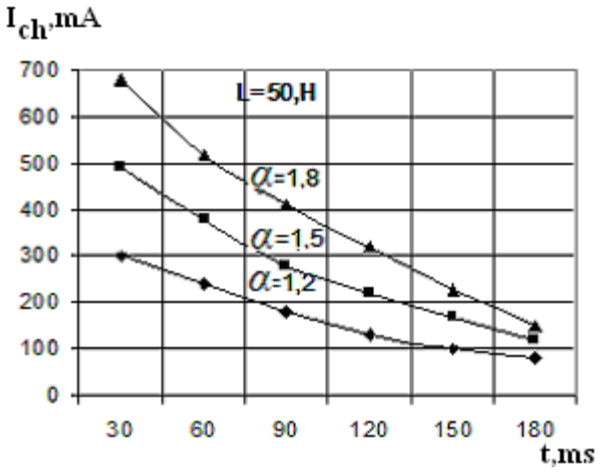


Fig.36

Influence of the conductivity angle and the time of the discharging process over the charging current and charging voltage

The curves from fig.35 to fig.39 refer to U_m=7,5 kV and parameters of the charging circuit mentioned above:R_1=3 kΩ; R_2=30 kΩ C_1=0,25 μF; C_2=1 μF.

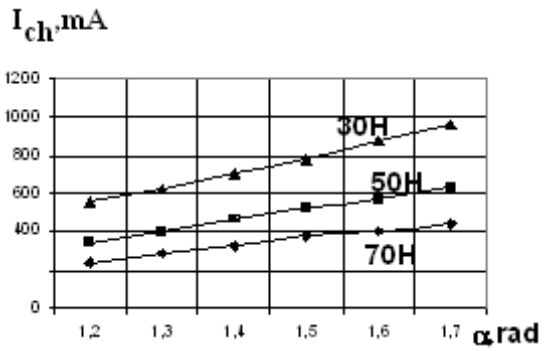


Fig.37

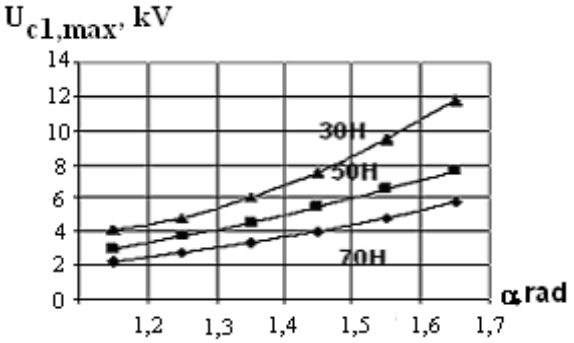


Fig.38

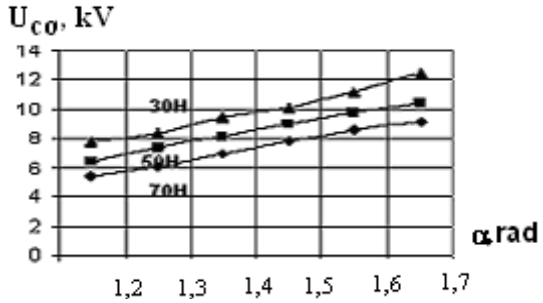


Fig.39

Influence of the conductivity angle and inductivity of the charging circuit over the maximum charging current and the voltage which C_1 and C are charging to

The work of the parallel stabilizer R_2, L_1, T_1, R_{L1} can be assessed from the graphics on fig.40, which refer to the repetition frequency of the discharge pulses: 0.2, 0.5, 1, 2, and 5Hz. P is the power dissipated by the parallel stabilizer. If the overcharging of the working capacitor battery C_2 is $U_{C2}>U_{C0}$ (U_{C0} – a preliminary defined value), then $P=0,5\ C_2(U_{C2}-U_{C0})\ (U_{C2}+U_{C0})f$, where f is the frequency of the power supply network. The graphs refer to the mode from fig.33 – U_{C2}=6 kW.

From everything pointed above it follows that for each certain charging circuit and mode (charging time and charging voltage) it can be defined a suitable conductivity angle of the symistor to ensure the both the mode and reduced loading of the elements in the charging circuit.

When switching on the parallel stabilizer, the conductivity angle decreases. Therefore it reduces the power dissipated by the parallel stabilizer. The discharge of the working capacitor is compensated at low frequency at the expense of the measuring circuits.

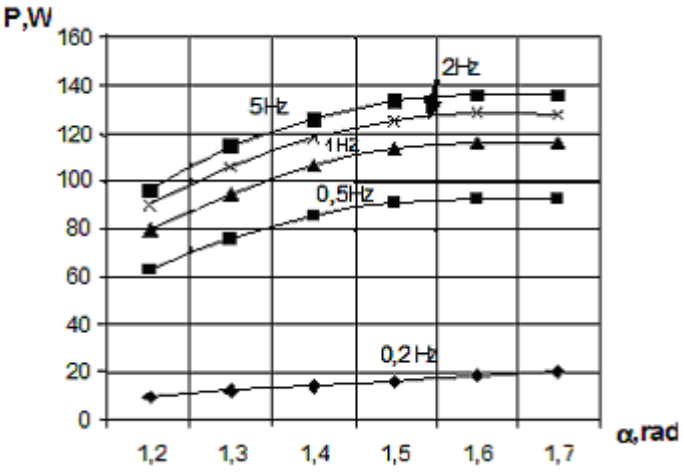


Fig.40 Dissipated power by the parallel stabilizer for compensation of the overcharge of the working capacitor

The discussed process can be divided into two periods:

- $U_{C2} < U_{C0}$ - capacitive energy storage;
- $U_{C2} \geq U_{C0}$ - stabilization process.

It is considered that the circuit is non-linear and $t_{ch} = t_{ch}(C_2, U_{C2}, U_m, \Delta U_m, \alpha)$, $i_{ch,\max} = i_{ch,\max}(C_2, U_m, \Delta U_m, \alpha)$ and $P = P(C_2, U_{C2}, U_{C0}, U_m, \Delta U_m, \alpha)$.

The analyzed schematic solution for the converter (including regulator for alternating voltage, step up transformer with dissipation; rectifying section with capacitive current-limiting element and parallel stabilizer) gives possibility for reduced current loading in the interval $U_{C2} < U_{C0}$ with a suitable choice of U_m and α and at the same time insures the controlled parameters t_3 and U_{C2}. In the period when $U_{C2} \geq U_{C0}$, the dissipated power is reduced with the change of α.

One variant of the scheme for control of the symistor switch is presented on fig.41.

The current generator T_4, D_{11}, D_{12} and R_{22}, R_{23} and transistor T_3

The triangular voltage is formed on C_2 by the current generator T_4, D_{11}, D_{12} and R_{22}, R_{23} and transistor T_3, which discharges C_2 when the supply voltage passes through 0. At this moment, the synchronized T_3 is triggered on by pulses which are formed by the Gretz scheme – $D_5 \div D_9$ and the comparator OA_3. The non-inverting amplifier OA_1 sets the comparison level with the triangular voltage. The conductivity angle can be regulating with VR1. The integrator R_1, C_1 integrates the pulses from p.1 - R_{L1} from the parallel stabilizer, when it switches on – fig.34. This leads to increasing the comparison level on the output of OA1 and decreases the conductivity angle of the symistor. OA2 is a comparator which compares the triangular voltage over C_2 and the output voltage of OA2. The formed pulses at the output of OA2 trigger on the optocoupler O_1 and after being amplified by transistor T_2 they control the symistor in the charging circuit. The light-emitting diodes D_3 and D_4 are used for visual control of the work of the scheme for symistor control.

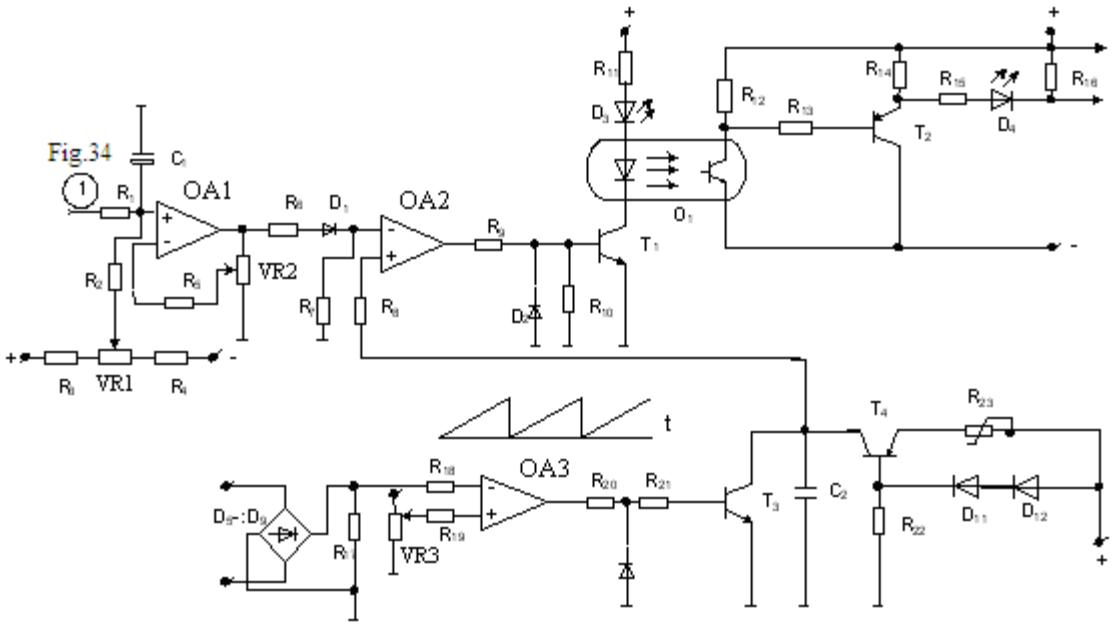


Fig.41 A scheme for control of the symistor switch in a doubler for capacitive energy storage

IV. RESULTS

It is proposed an unified schematic solution for a converter in the circuit for capacitive energy storage. It includes AC regulator, step-up transformer with dissipation, rectifying section with reactive load and parallel stabilizer, which meets the requirements for work both in the high-voltage and low-voltage circuits, where:

- two control circuits are formed – AC regulator on the input and compensation stabilizer on the output. This gives possibility for independently setting of two of the controlled parameters in a wide range – the charging time and the charging voltage of the capacitor battery for ensuring instability of 1% of this voltage and reduced loading of both the converter elements and the input supply network.
- the charging time is divided in two periods – increasing of the voltage over the capacitor battery and its stabilization. It is proposed a schematic solution for control of the symistor switch, which ensures correction of the conductivity angle during the stabilization mode and following decrease of the dissipated power by the parallel stabilizer.

For a non-linear circuit of the converter including also unusual rectifying sections with capacitive reactive load is suggested a mathematical model – a system of differential equations. It is solved with MATLAB which allows computer visualization of the processes of capacitive storage and stabilization where:

  - the controlled parameters (charging time, charging voltage and its instability) and the requirements to the elements of the converter circuit are more accurately defined by including more influencing parameters and the specifics of the charging circuit.

- the suggested model follows to be accepted as a methodology for design

The analytically obtained results are compared with experimental ones from a certain prototype for formation of pulse discharge in liquid medium. There is good matching between the two types of results while considering the non-linear character of the processes in the device and the presence of magnetic circuits.

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